
Intel
Developer
Forum
Fall 2002
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Advancing the Digital Universe

Welcome to the Intel Developer Forum Conference Fall 2002

Frank Spindler
Vice President
Corporate Technology Group

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Compaq iPAQ* Handheld

- Win a Compaq iPAQ* Handheld Computer
- Drawing at 8:00 a.m. Tuesday and Thursday
- Prize to be awarded at that time
- Get your raffle ticket at door of keynote room
- Tickets valid for same day drawing only

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*Other names and brands may be claimed as the property of others

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Fall IDF 2002 is Wireless

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*Other names and brands may be claimed as the property of others

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Fall IDF is Wireless!

- 802.11a and 802.11b wireless LAN coverage in concourse & session rooms
- Available for laptops and Pocket PC* devices
- Free internet access!
- Wireless cards and Compaq* iPAQ PDAs for sale at the wireless connectivity solution center (concourse level)

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Be connected "anytime, anywhere"

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Save the Date - Spring IDF 2003

February 18-21, 2003

San Jose, CA

Fill Out a Conference Survey!

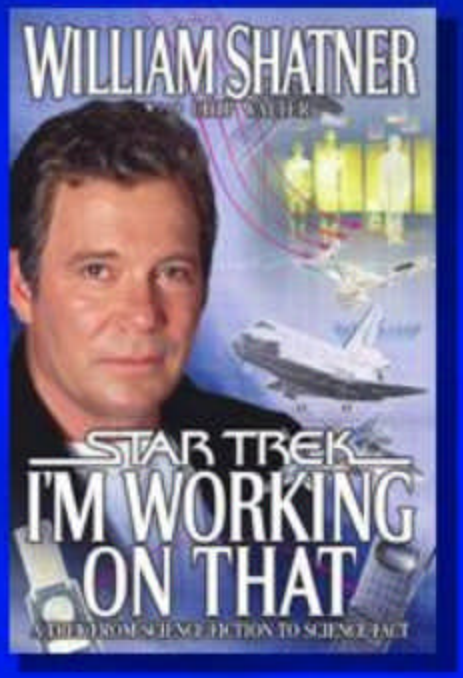
- Win a Free T- shirt
- We want your opinion.
  Help us improve IDF
- Fill out a survey at the Registration Booth

Intel Developer Update (IDU)

- FREE online monthly developer magazine
- Technology Articles
- www.intel.com/update

See William Shatner at IDF!

- Q&A session (not a book signing) with William Shatner and Chip Walter
- Authors of *Star Trek: I'm Working on That: A Trek from Science Fiction to Science Fact*
- Buy the book at the IDF Bookstore



Thursday 8:00 a.m. at Keynote and
Thursday 12:00 – 1:00 p.m.
Room B, San Jose Convention Center

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Building the Digital Future

Pat Gelsinger
Chief Technology Officer
Vice President
Corporate Technology Group

Sunlin Chou
General Manager
Senior Vice President
Technology & Manufacturing Group

September 12, 2002


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Yesterday's Dreams
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Discovering Pathways

Alan Kay

"The best way to predict the future is to invent it."

"Nanotechnology offers... possibilities for health, wealth, and capabilities beyond most past imaginings "

Eric Drexler

Neil Gershenfeld

"... our goal is to embed intelligence into everyday objects... "

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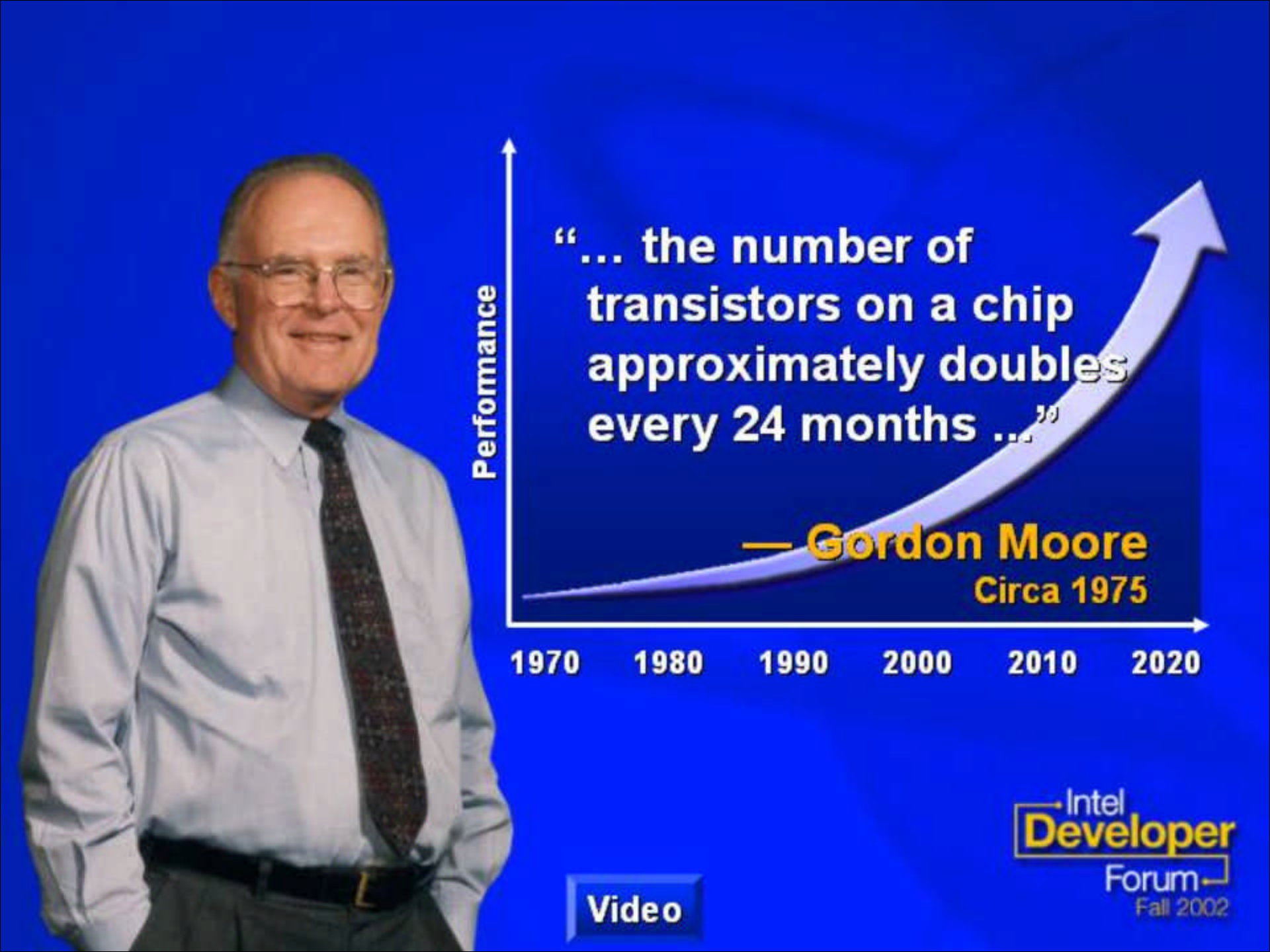
Perfomance
"... the number of transistors on a chip approximately doubles every 24 months ..."
— Gordon Moore
Circa 1975
1970
1980
1990
2000
2010
2020
Video
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The Digital Future

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Bridge to the Digital Future

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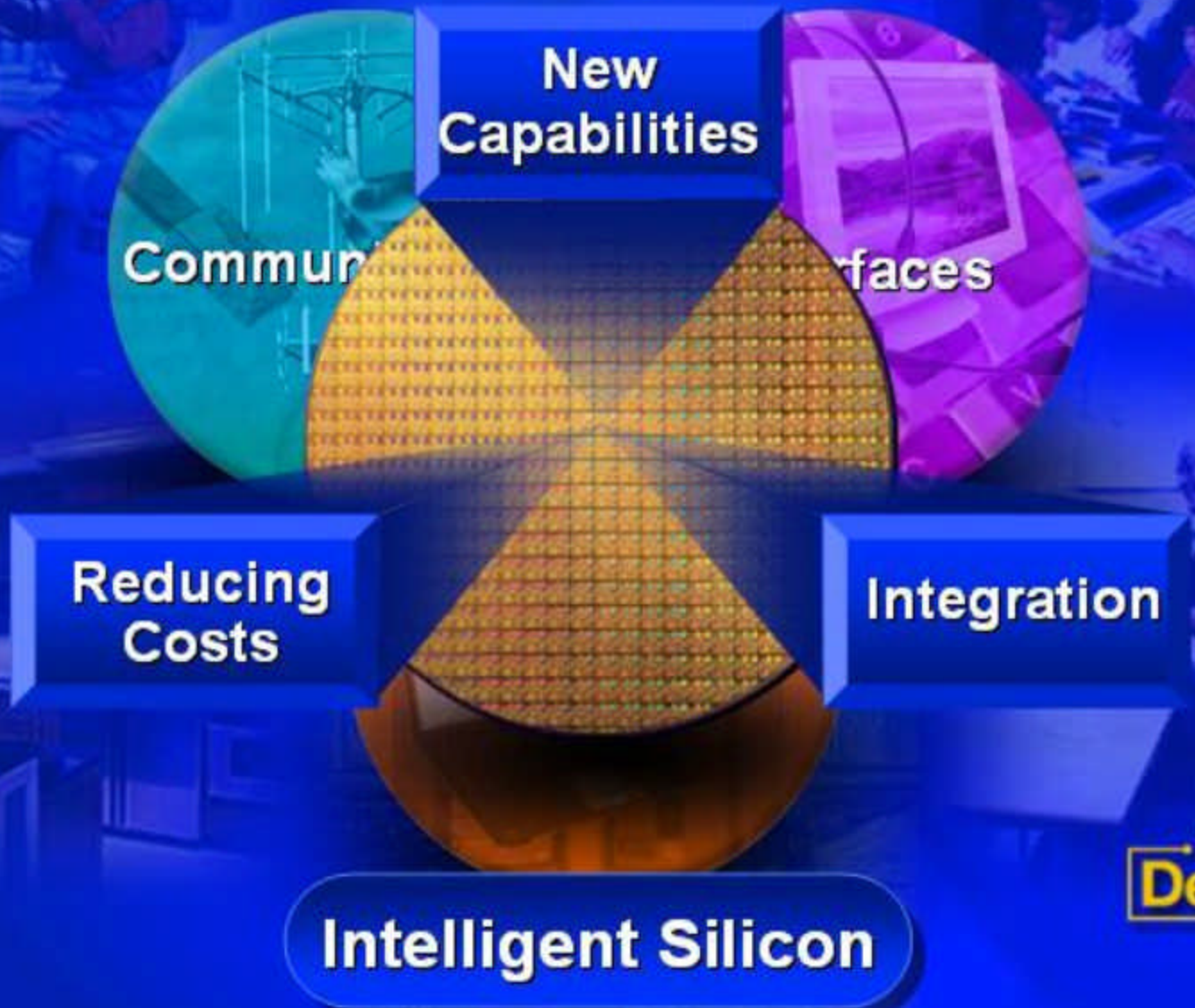
Silicon: The Underlying Trajectory



Moore's Law: Industry Guidepost

EXTENDING

Discrete

Moore's Law: Industry Guidepost

EXTENDING

Discrete SSI

Moore's Law: Industry Guidepost

Moore's Law: Industry Guidepost

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Moore's Law: Industry Guidepost

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“Radio Free Intel”

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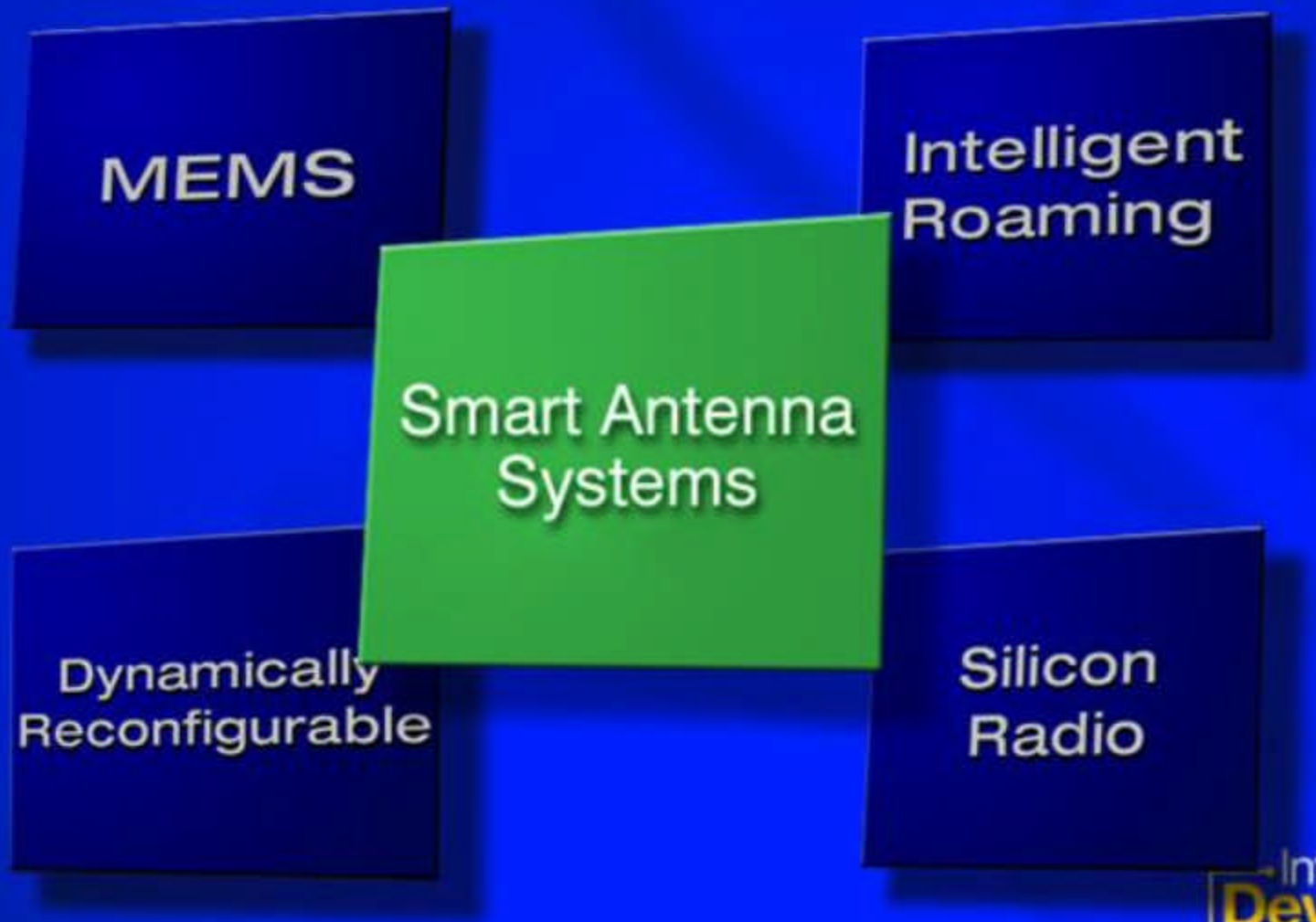
"Radio Free Intel": Research Areas



Smart Multiple-Antenna Systems

Complex Scheduling/Encoding	Signal Processing Antenna Control	Benefits
Spatial Frequency Time	Phase Amplitude	Capacity Throughput Coverage Reliability


Silicon Photonics

TODAY

Silicon Electronics

Moore's Law
– Intel Does it Best

Silicon
Processor

RESEARCH

Silicon Photonics

Silicon-based Optical
Building Blocks

- WAVE GUIDES
- FILTER
- MODULATOR
- FAST SWITCH
- PHOTO DETECTOR

Integrated Electronics and Photonics

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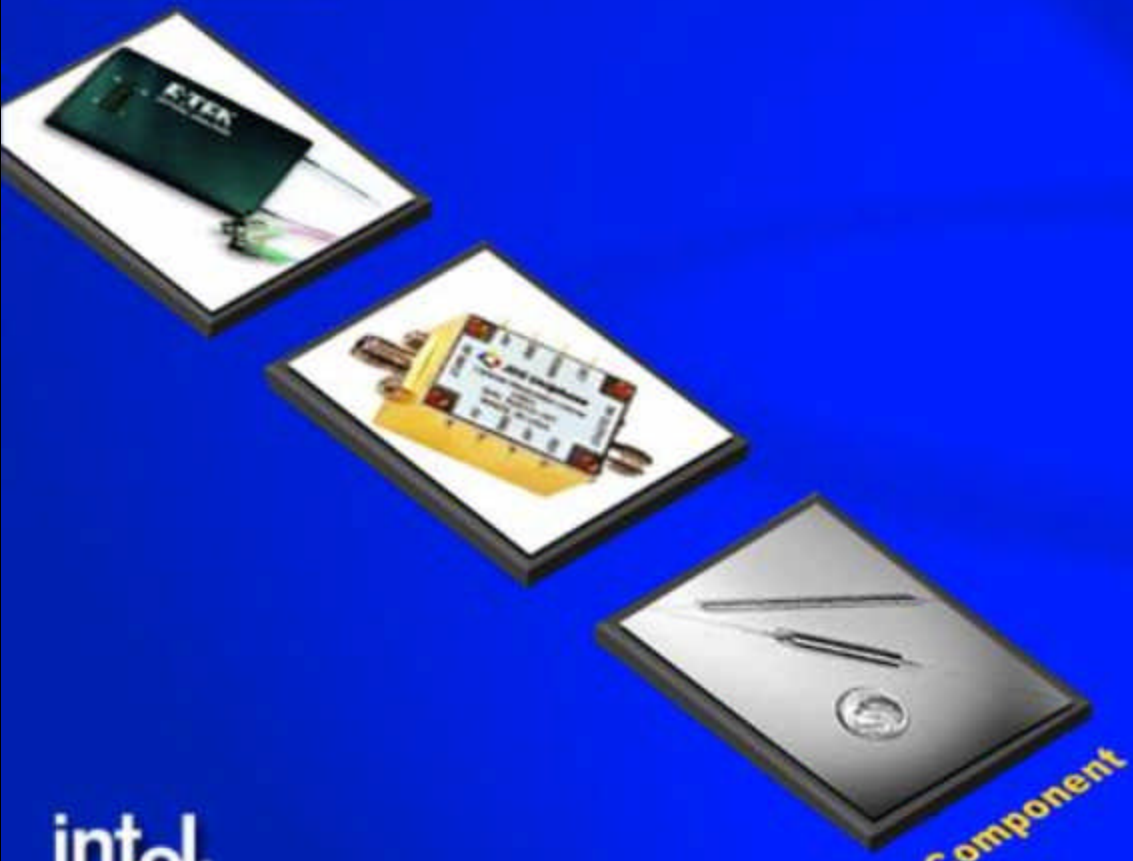
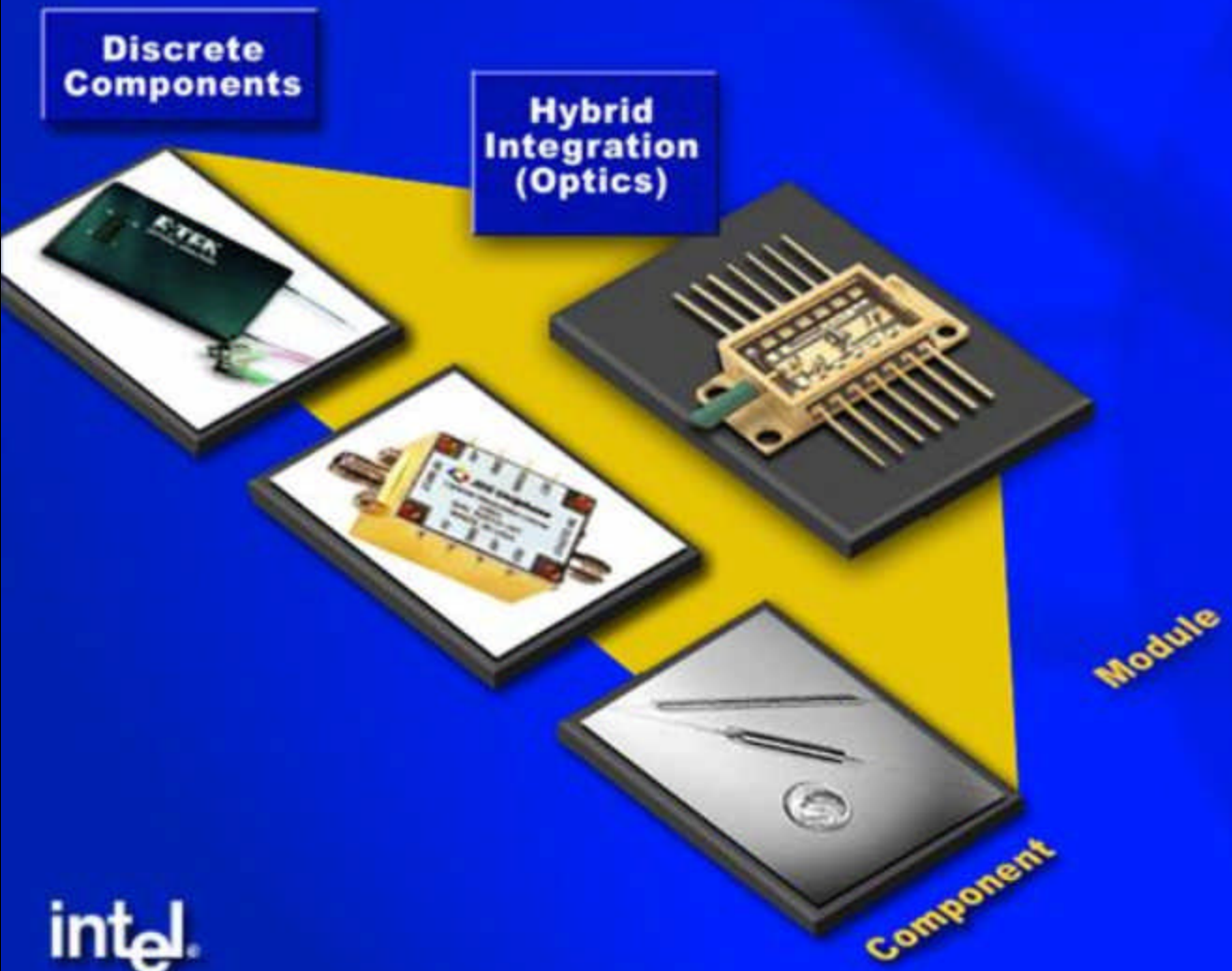
Next Steps: Integration Phases

Discrete Components



Component

Next Steps: Integration Phases



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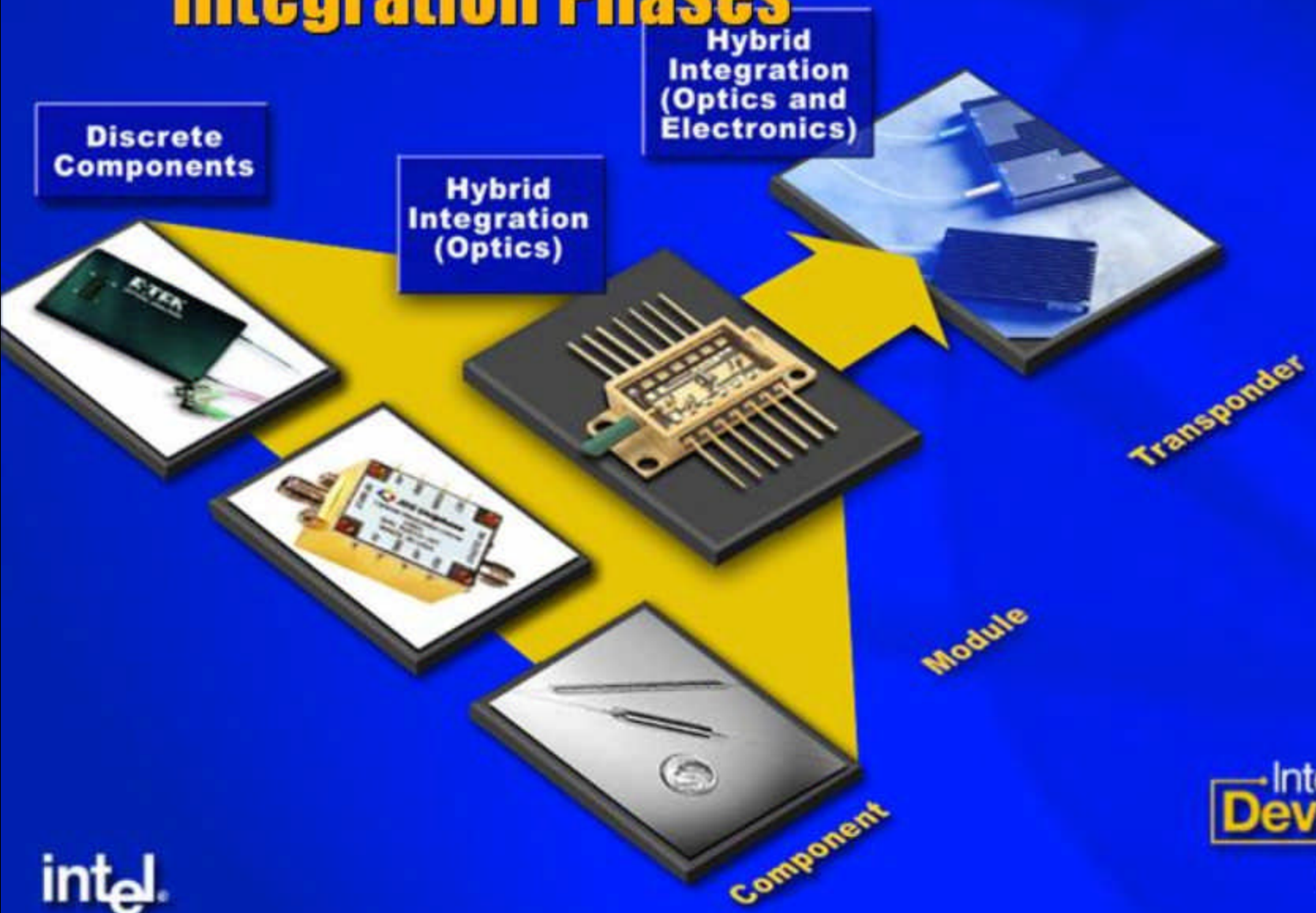
Next Steps: Integration Phases



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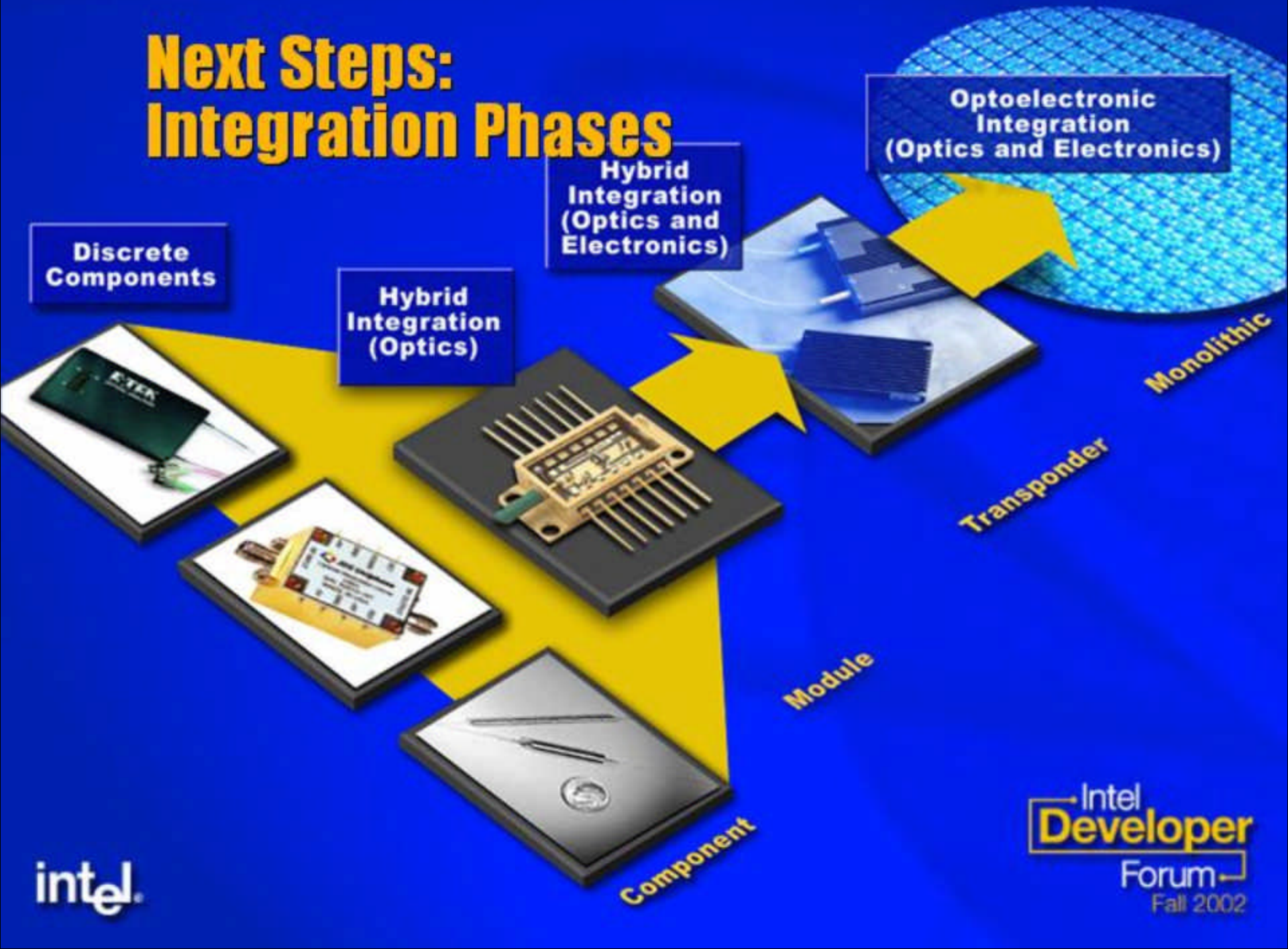
Next Steps: Integration Phases



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Sensor Networks

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Sensor Networks

Sensing +

Computing +

Communicating

Communications-Computing

Great Duck Island Deployment

Great Duck Island

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Demo

Fall 2002

Programming Sensor Networks Research

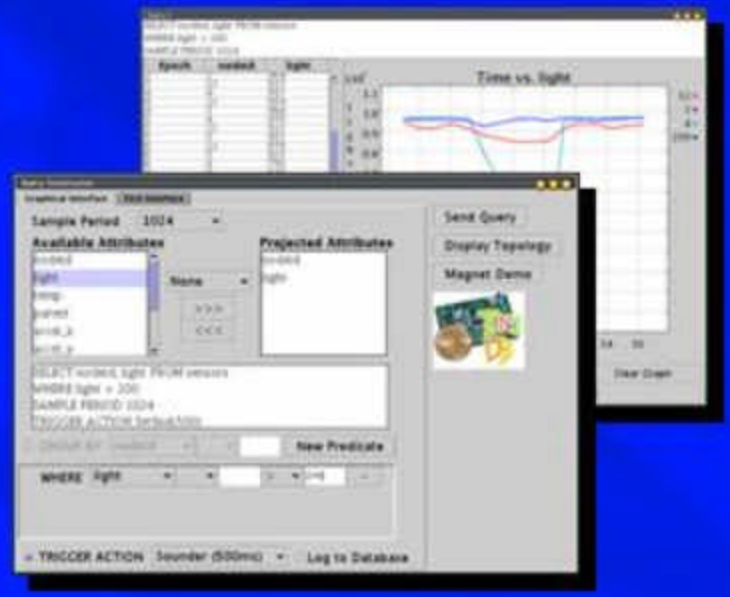
TinyOS

a component-based OS for the networked sensor regime

http://webs.cs.berkeley.edu

Berkeley

University of California



http://berkeley.intel-research.net/tinydb/

TinyDB: In-Network Query Processing in TinyOS

Samuel Madden, Joe Hellerstein, and Wei Hong

IRB-TR-02-014

August, 2002

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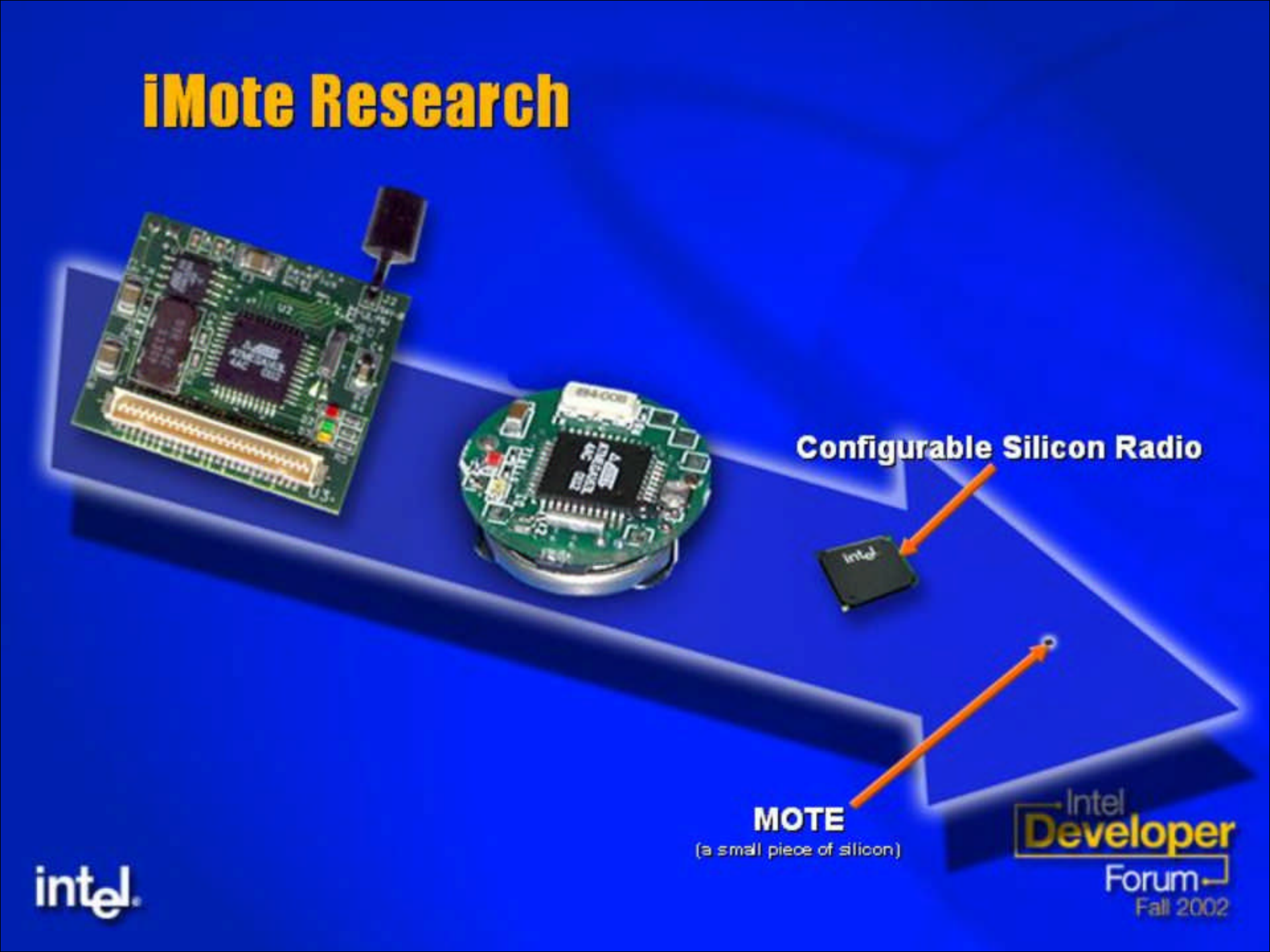
iMote Research



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Silicon Trajectory

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What is Nanotechnology?

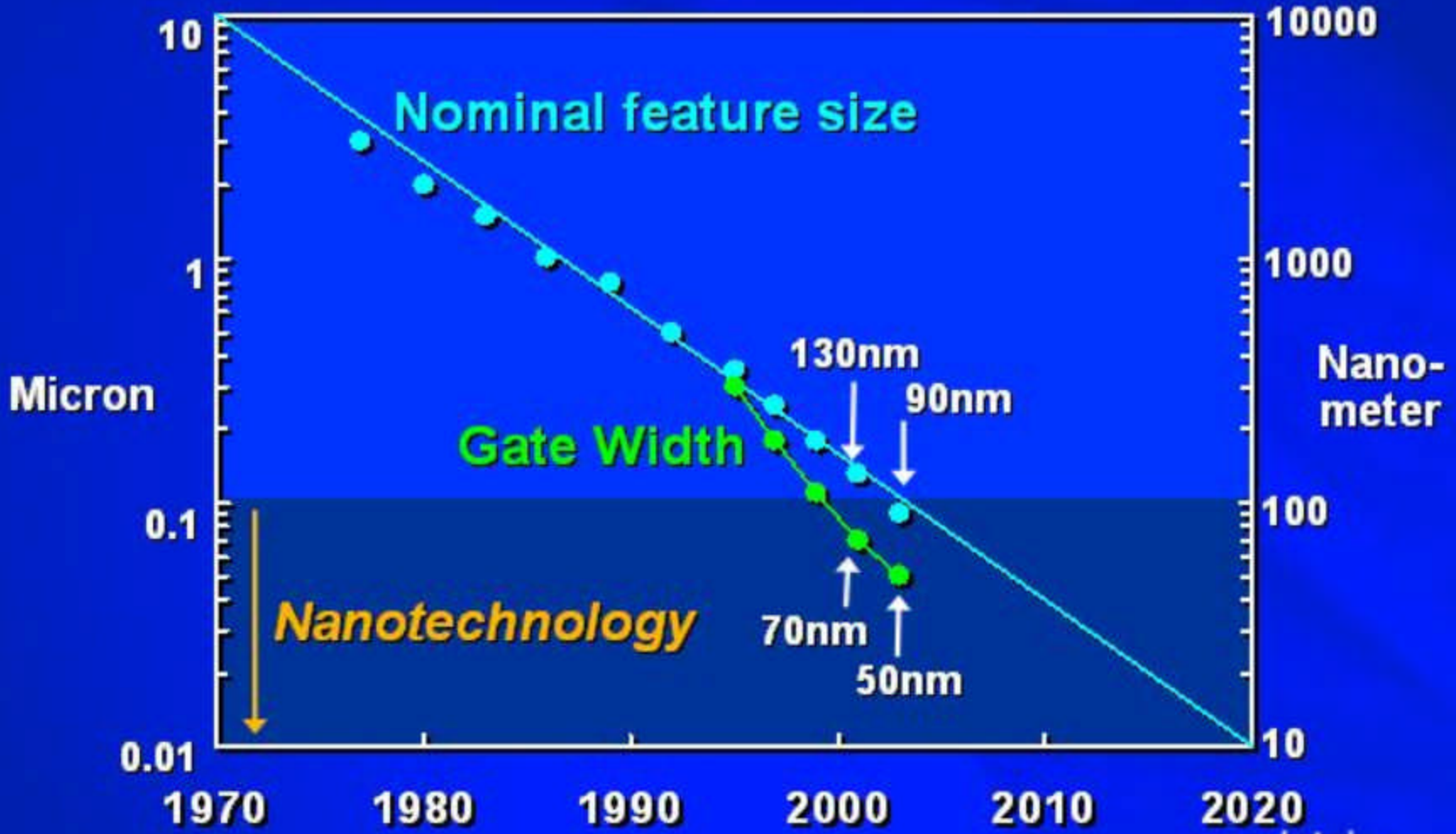
a. New structures like carbon nanotubes
b. Silicon devices made smaller
c. Arranging atoms and molecules
d. Letting atoms assemble themselves
e. Something far in the future
f. In production today
g. All of the above

Correct answer: g.

Nanotechnology features

- Structures measured in nanometers
  - Less than 0.1-micron (100nm)
- New materials and device structures
  - Incrementally changing silicon technology base
- Materials manipulated on atomic scale
  - In one or more dimensions
- Increasing use of self-assembly
  - Using chemical properties to form structures

Silicon Nanotechnology is Here!



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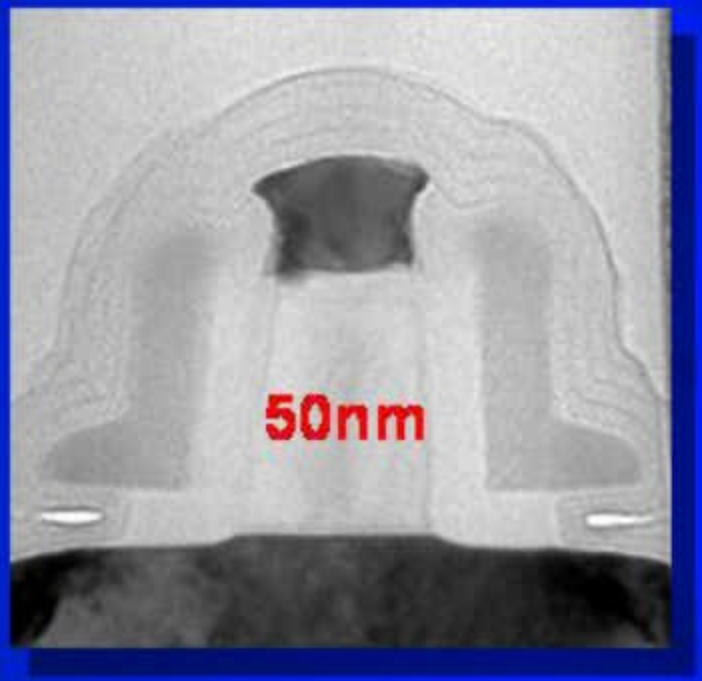
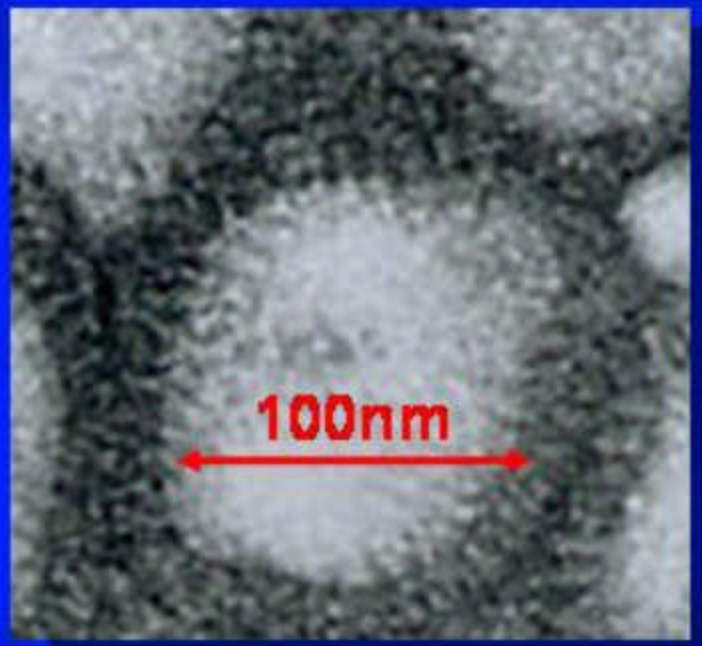
Silicon Devices Shrink to Virus Size



Transistor for 90nm Process

Source: Intel



Influenza virus

Source: CDC

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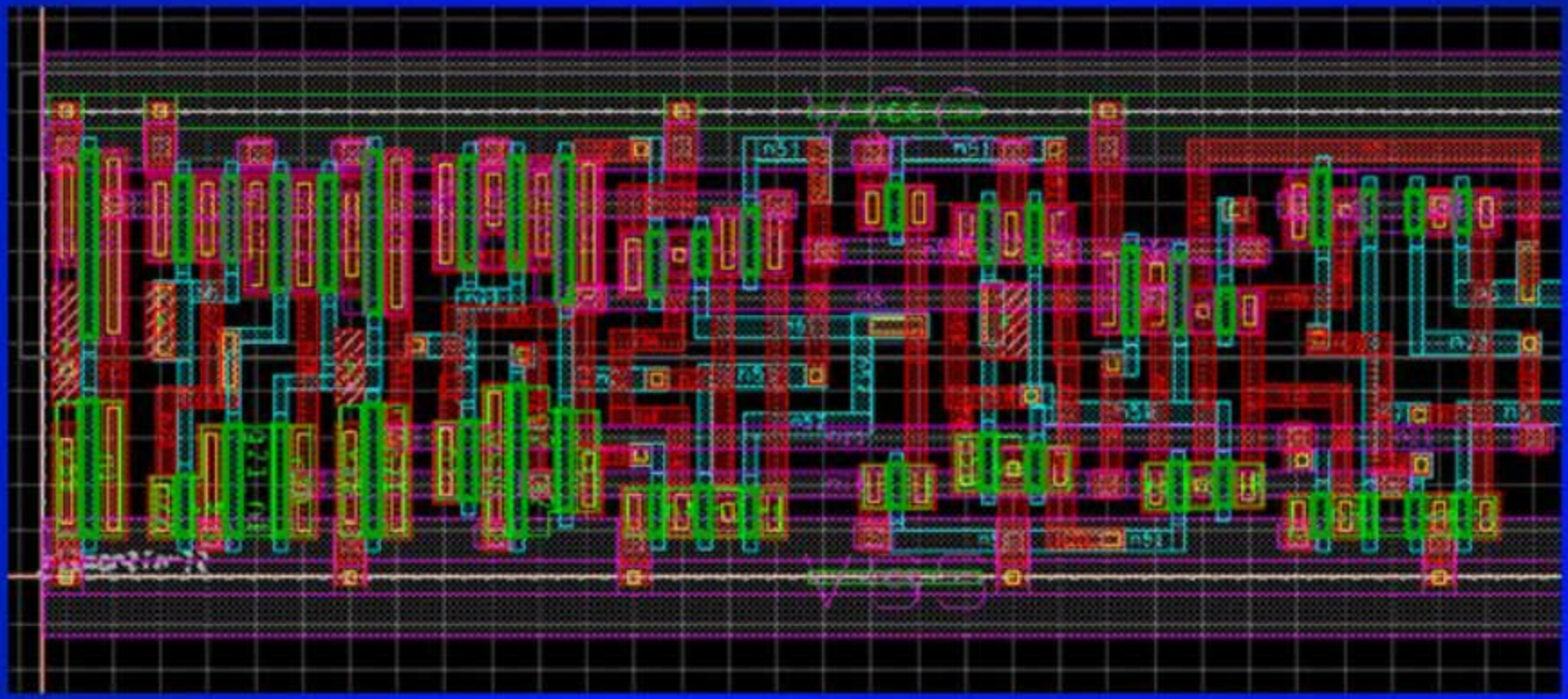
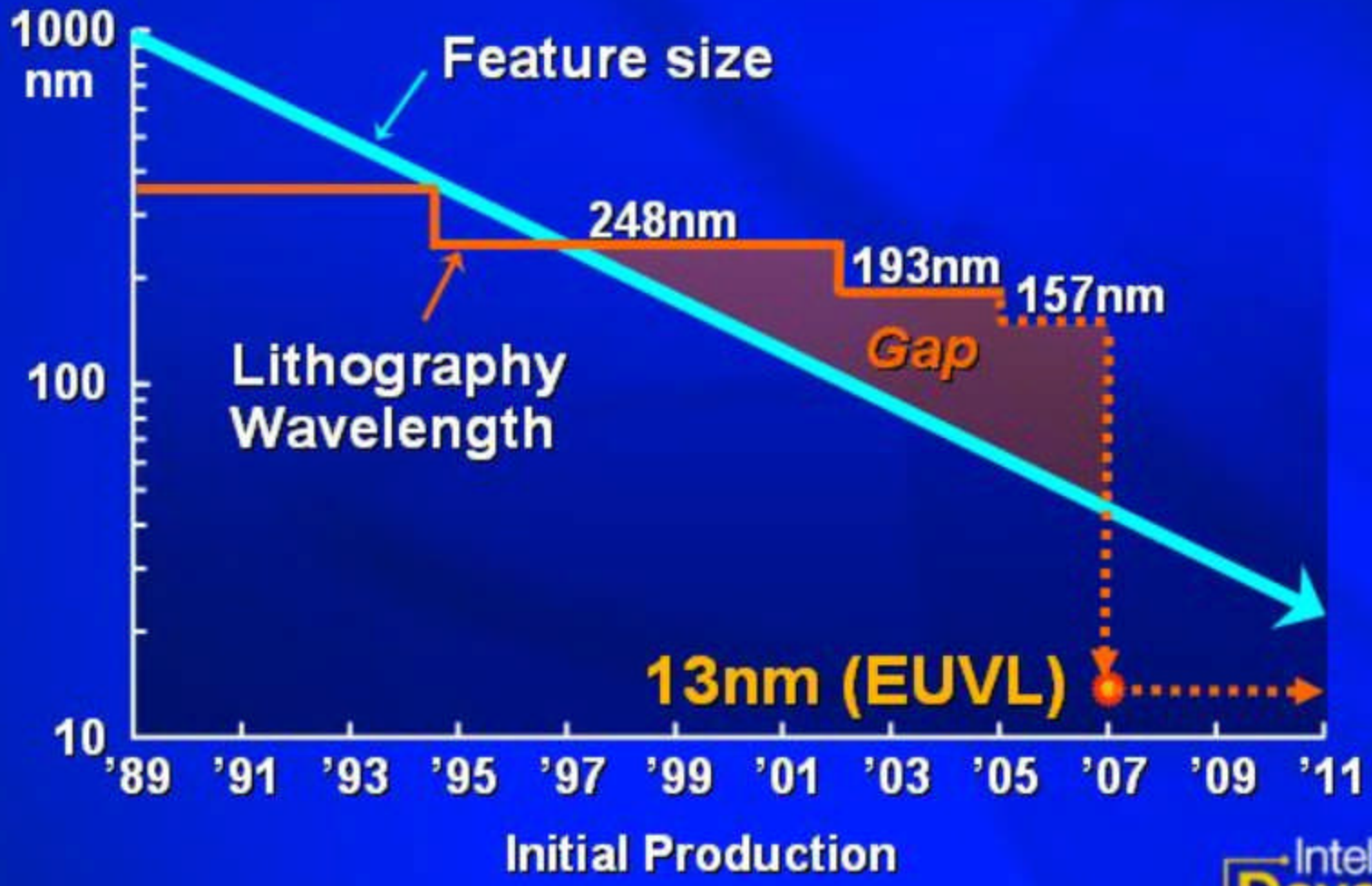
Lithography is the Designer's "Brush"

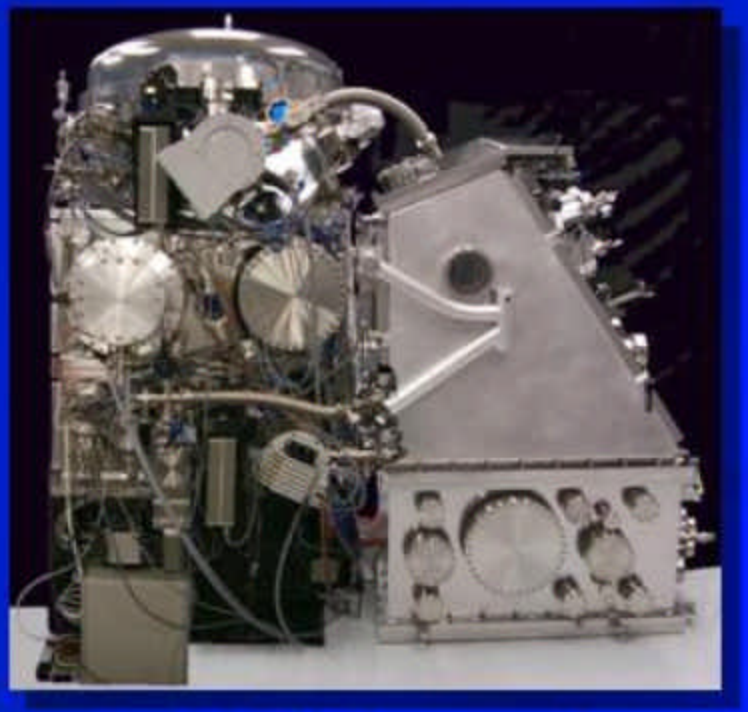


Lithography is indispensable for defining locations/configurations of circuit elements/functions

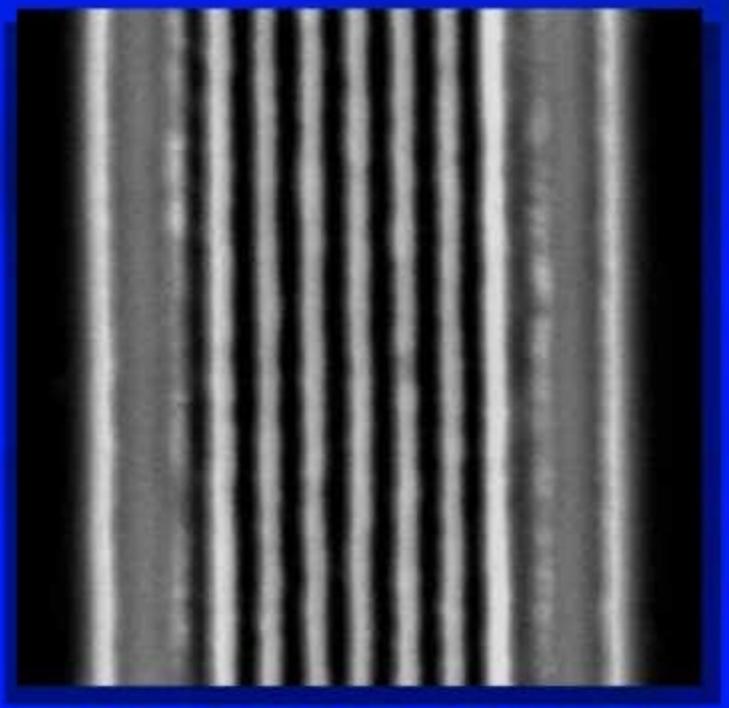
Lithography Gap to Close with EUVL



EUV LLC Consortium Demonstrates EUVL



EUV Lithography Prototype Exposure Tool



50nm Lines Printed with EUV Lithography

Source: Sandia

EUV lithography is now in commercialization phase

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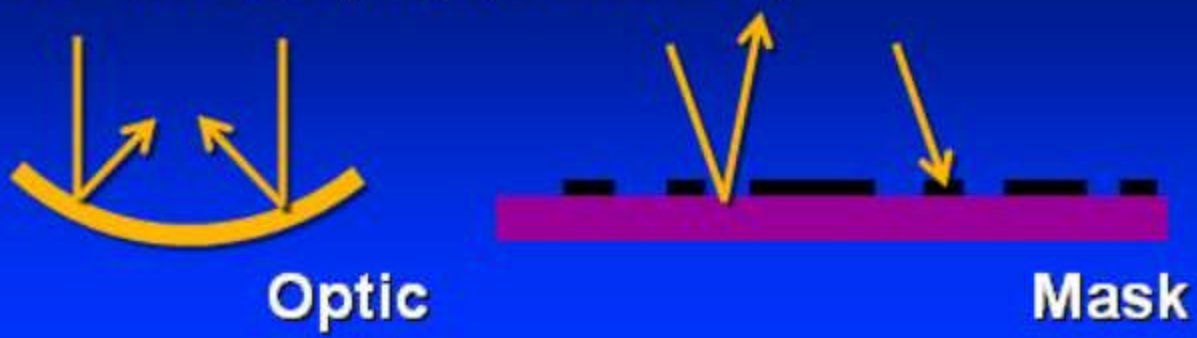
EUVL Overcomes Optical Materials Limits

Conventional lithography (refractive)

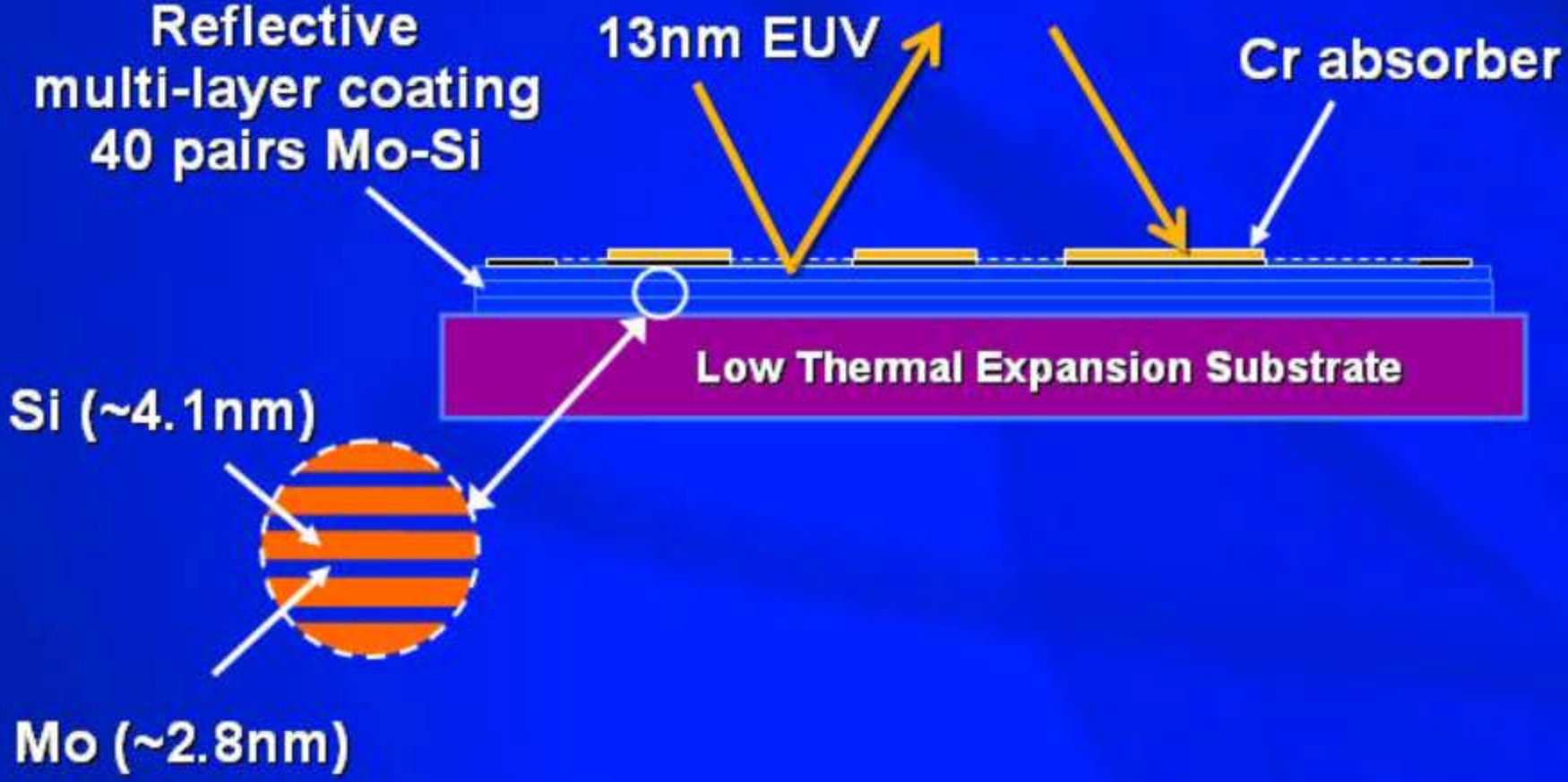
Optical materials do not transmit short wavelengths

EUV lithography (reflective)



Multi-layer coating reflects short wavelengths

EUV Reflective Mask Structure



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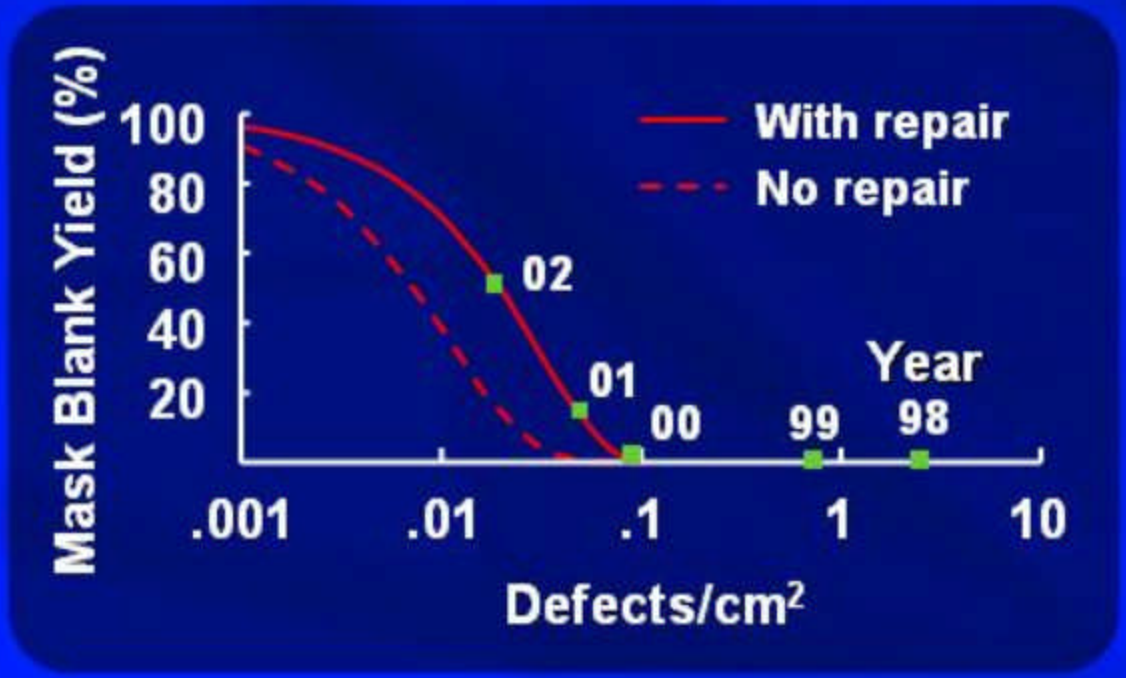
EUV Mask Yield Breakthroughs

EUV Mask



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New Materials, Devices Extend Si Scaling

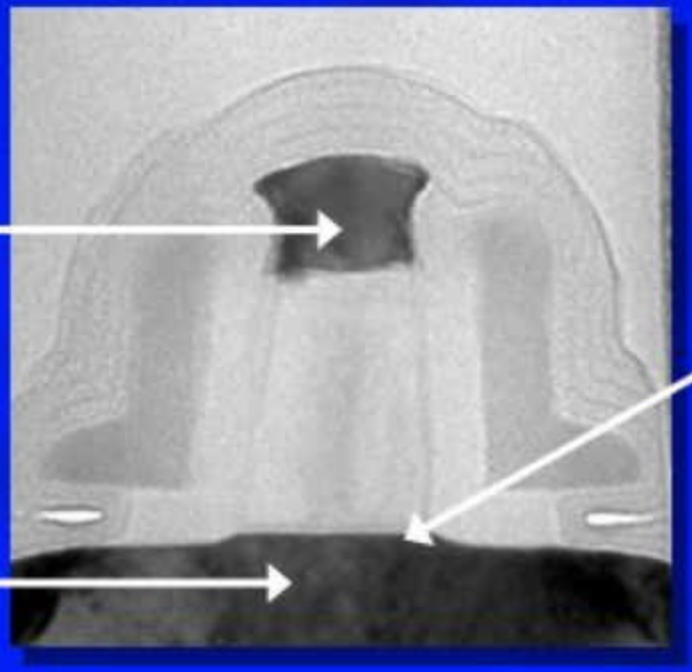
Changes Made

Gate

Silicide added

Channel

Strained silicon



Transistor

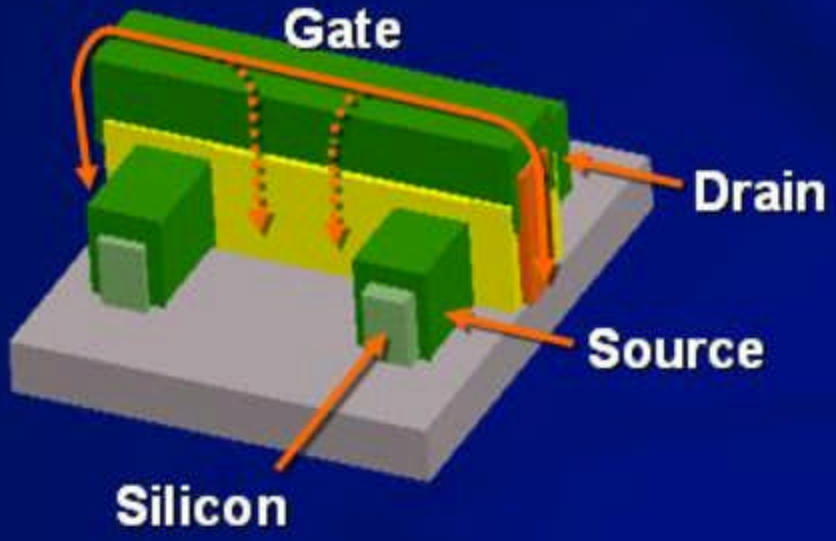
Future Options

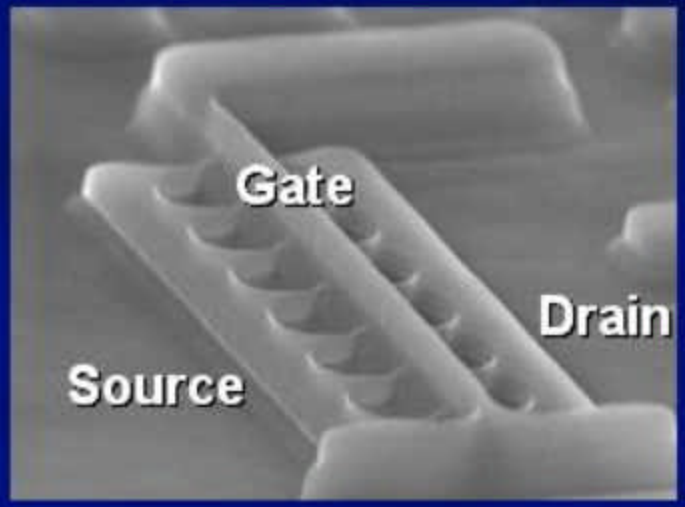
High-k gate dielectric

New transistor structure

Source: Intel

Experimental Tri-Gate Transistor





Source: Intel

- Improved version of TeraHertz transistor
  - Better performance
  - Scalable to smaller sizes
- Technical details to be presented
  - ISSDM Conference, Japan, Sept 17, 2002

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New Materials, Devices Extend Si Scaling

Changes Made

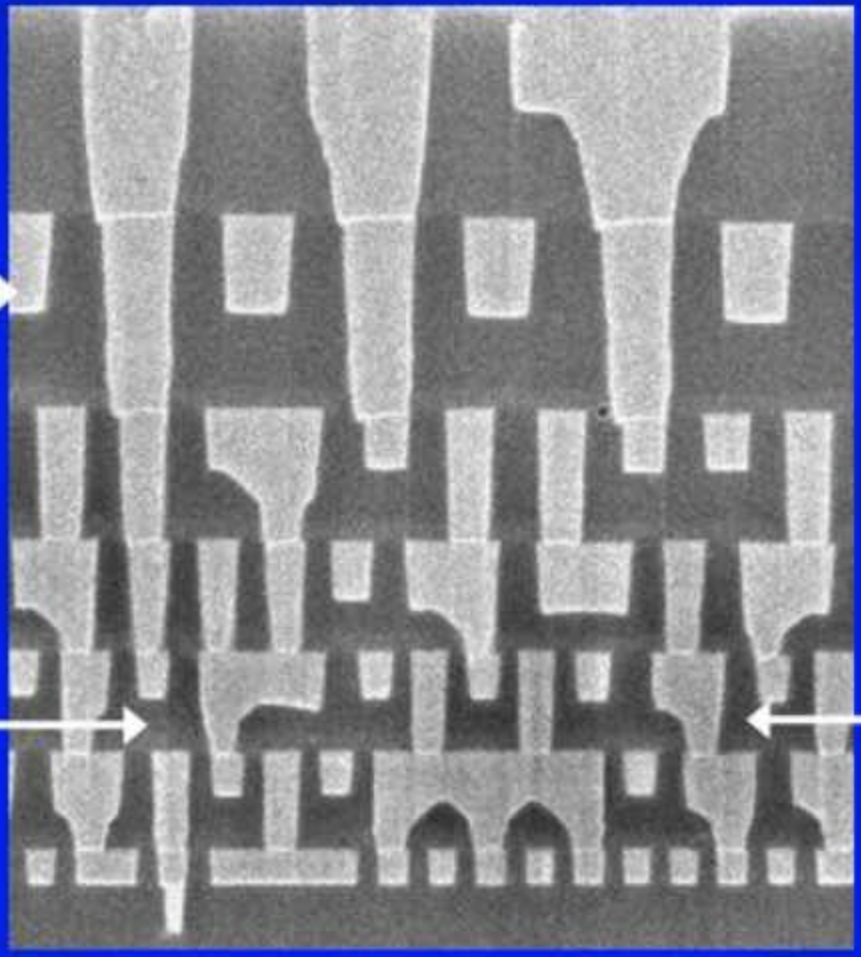
Metal lines

Al → Cu

Insulating dielectric

SiO_2 → SiOF

→ CDO (low-k)



Future Options

Ultra Low-k Dielectric

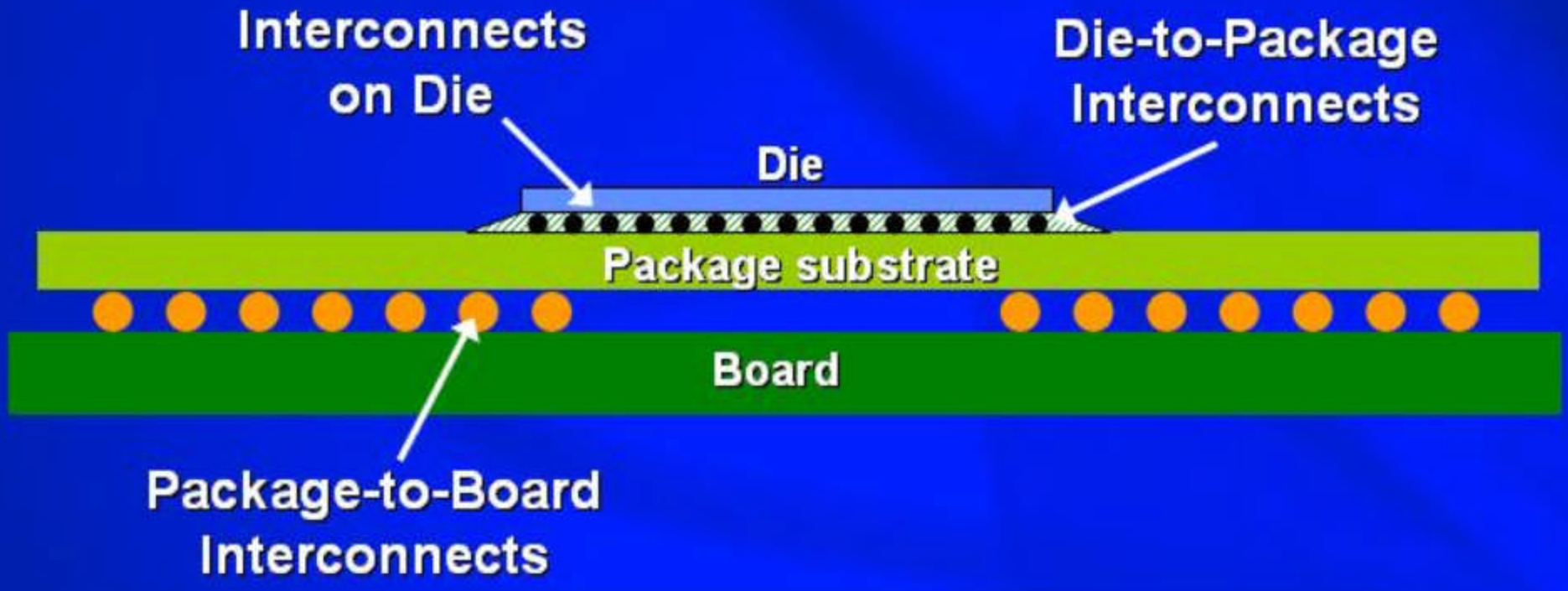
Interconnects

Source: Intel

intel

Die/Package Integration More Critical

Points of Vulnerability:

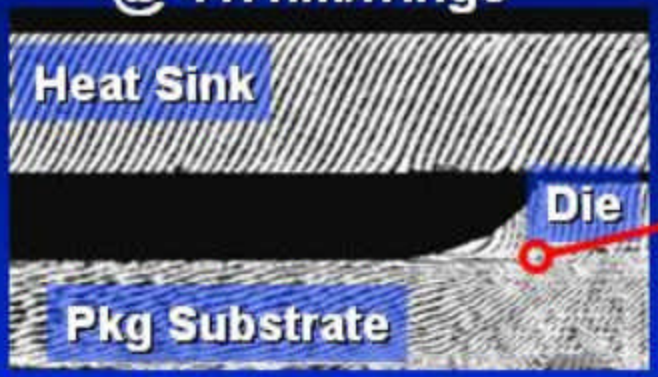


Materials and structures must withstand thermal-mechanical stresses

Analytical Tools For Nanotechnology

Package/Interconnect Deformation Measurements

Conventional Moiré @ 417nm/fringe

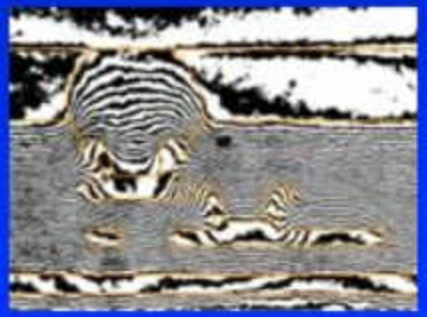


V-field (Vertical Displacements)

U-field (Horizontal Displacements)

Micro-Moiré @ 52 nm/fringe

U-field (Horizontal)



V-field (Vertical)

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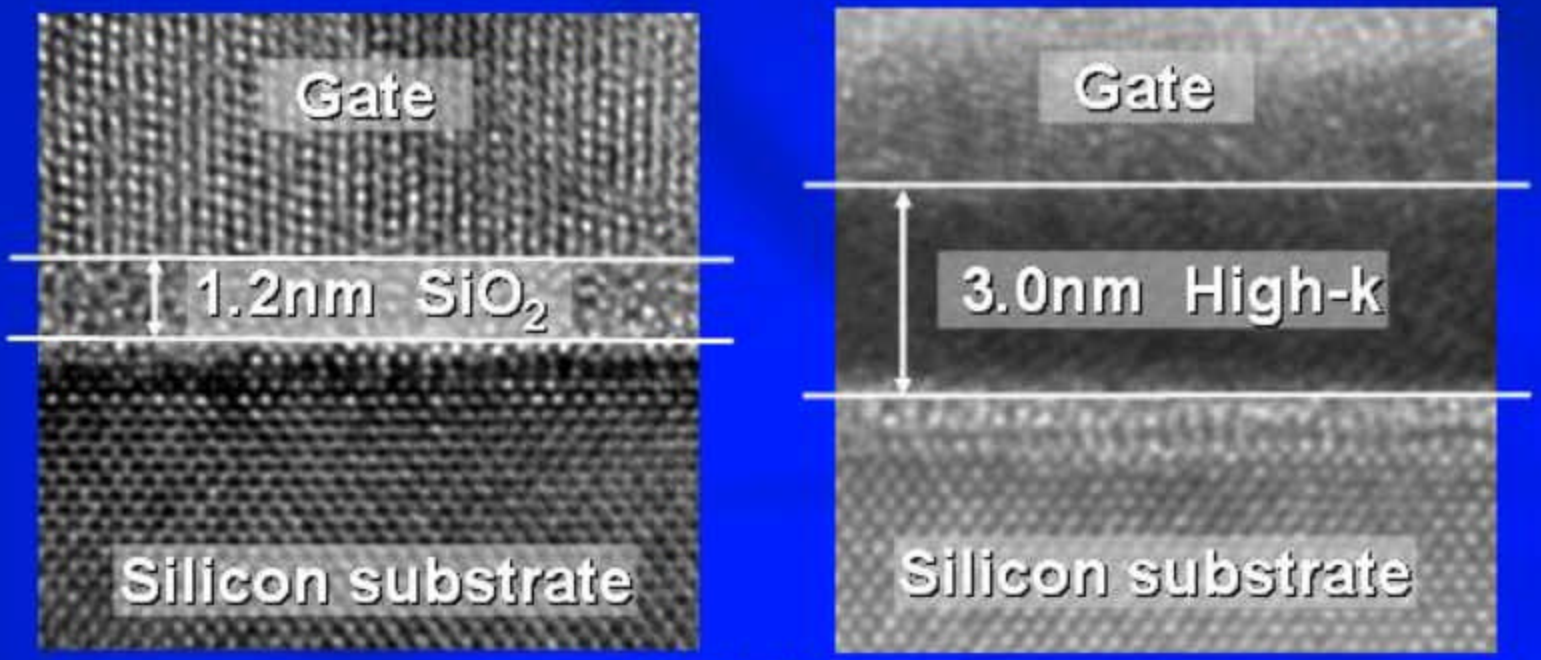
Source: Intel

Nanotechnology for Gate Dielectrics

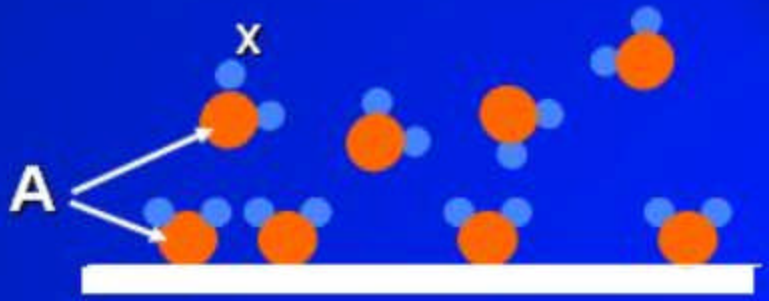


Source: Intel

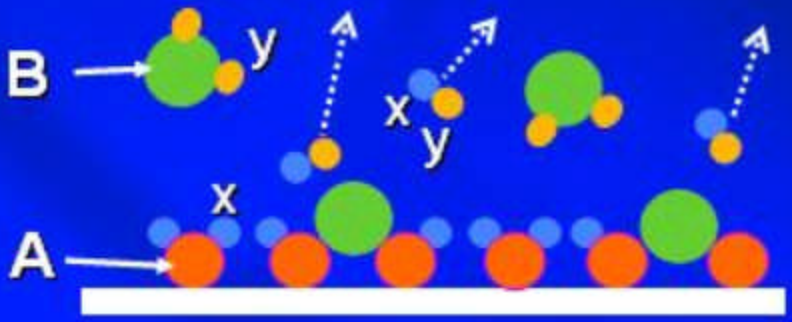
	90nm process	Experimental high-k
Capacitance	1X	1.6X
Leakage	1X	< 0.01X

Integration is the key challenge

Crafting Films with Atomic Layer Deposition



Step 1



Step 3

Step 2

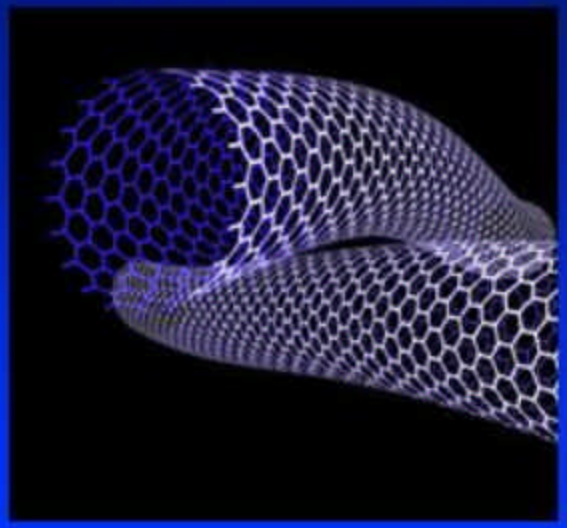
Step 4

ALD: Today's nanotechnology for self-assembly by atomic layer

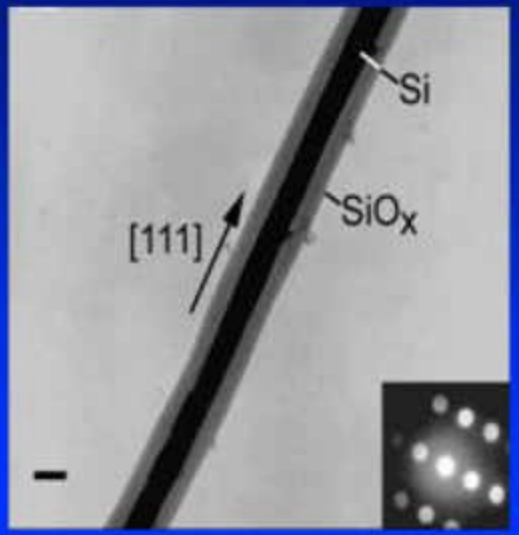
Nanotechnology Futures (> 2010 ?)

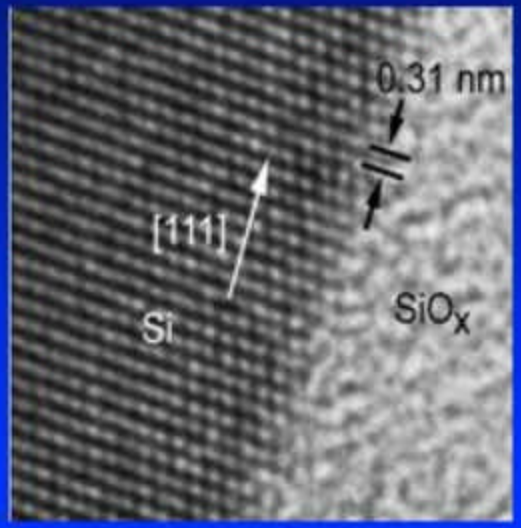
- Many options including nanotubes/nanowires
- Collaborations with universities in progress

Carbon Nanotube



Silicon Nanowire





Source: Morales & Lieber, Science **279**, 208 (1998)

Intel Involved in University Research

Intel-supported Nanotechnology Research at Universities

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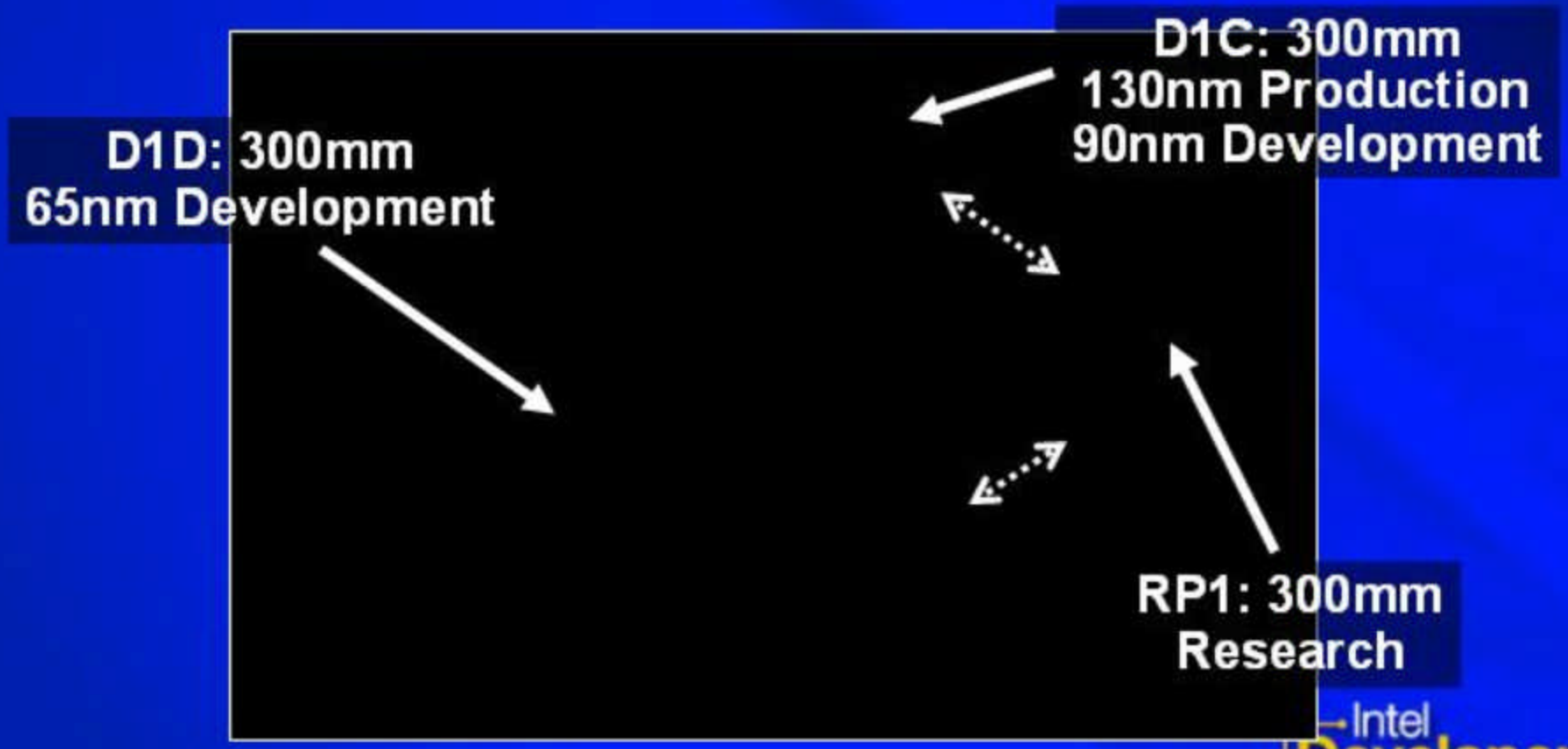
Speeding Nanotechnology to Production

Linking 300mm Research, Development, Production



Source: Intel

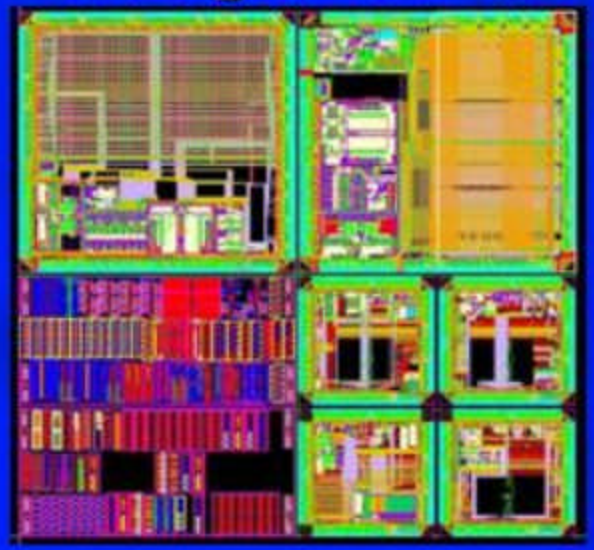
Nanotechnology for Computing and Communications

Process Development Test Vehicles

52Mb SRAM

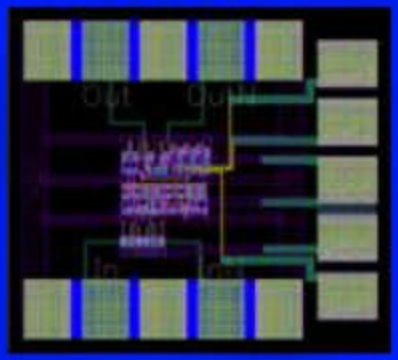
For Processors

WCDMA
Analog/RF circuits



For Wireless (Cellular)

40 Gb/s SiGe test circuit

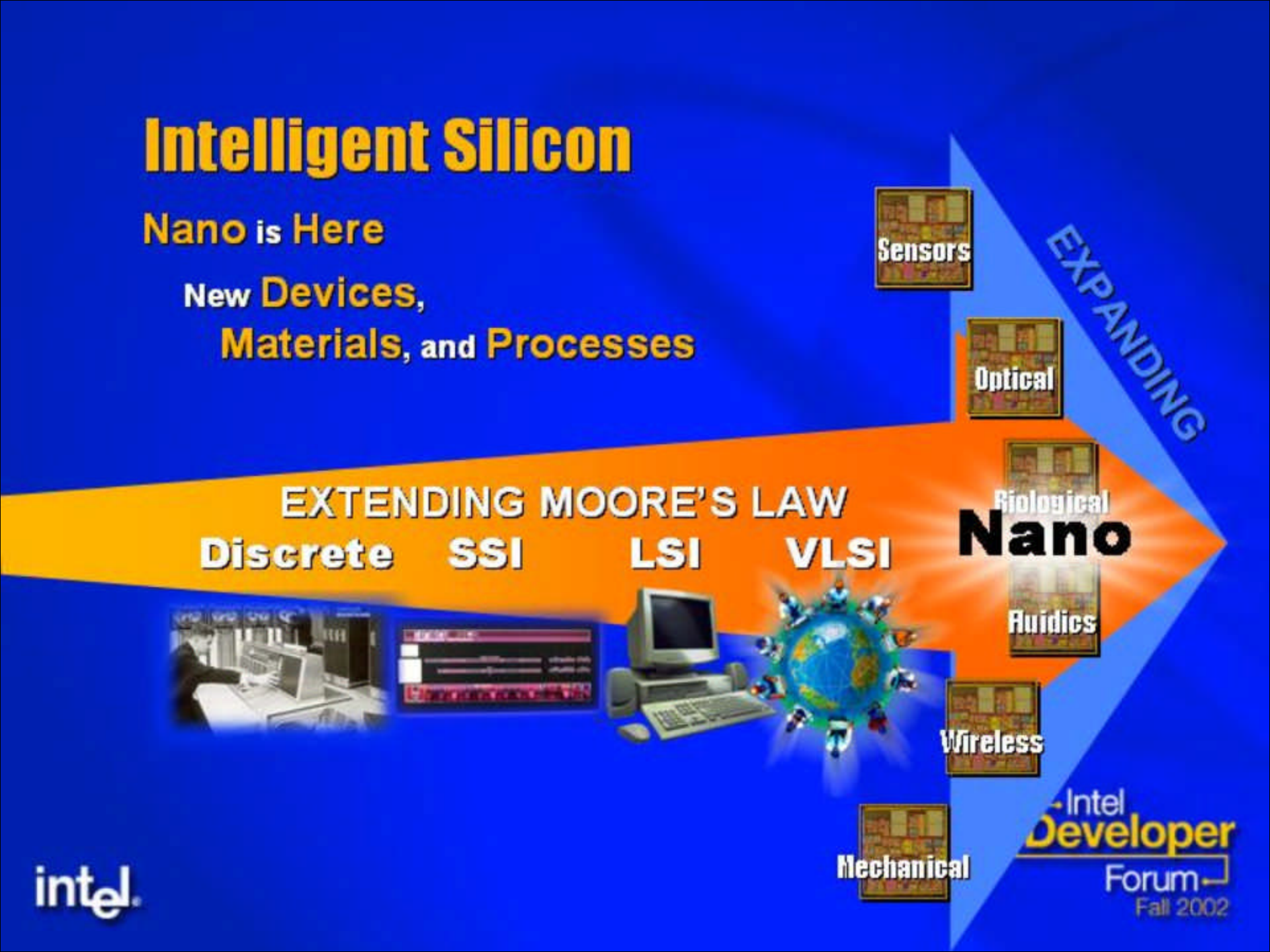


For Optical Communications

Intelligent Silicon

Nano is Here

New Devices,
Materials, and Processes



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Nano is Here

New Devices,
Materials, and Processes

Expanding the Silicon Canvas

EXPANDING

Sensors

Optical

Biological

Nano

Fluidics

Wireless

EXTENDING MOORE'S LAW

Discrete SSI LSI VLSI

Silicon Innovation Enabling Convergence

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A Piece of Nanotechnology

EUV mask

80-layer EUV reflective coating
on thin substrate

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